

MEMORY

4 M × 32 BIT HYPER PAGE MODE DRAM MODULE

MB8504E032AA-60/-70

4 M × 32 Bit Hyper Page Mode DRAM Module, 5 V, 1-bank

■ DESCRIPTION

The Fujitsu MB8504E032AA is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of eight MB8117405A devices. The MB8504E032AA is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8504E032AA are the same as the MB8117405A which features hyper page mode operation providing extended valid time for data output and higher speed random access of up to 2,048 bits of data within the same row than the fast page mode. For ease of memory expansion, the MB8504E032AA is offered in a 72-pad Single In-line Memory Module package (SIMM).

■ PRODUCT LINE & FEATURES

Parameter		MB8504E032AA-60	MB8504E032AA-70
RAS Access Time		60 ns max.	70 ns max.
Random Cycle Time		104 ns min.	124 ns min.
Address Access Time		30 ns max.	35 ns max.
CAS Access Time		15 ns max.	17 ns max.
Hyper Page Mode Cycle Time		25 ns min.	30 ns min.
Power Dissipation	Operating Mode	4620 mW max.	3960 mW max.
	Standby Mode	44 mW (CMOS) / 88 mW (TTL)	

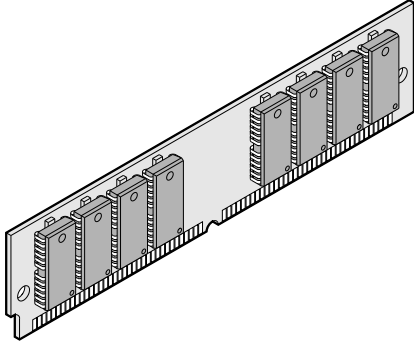
- Organization : 4,194,304 words × 32 bits
- Memory : MB8117405A, 8 pcs
- 5.0V ±10% Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Hyper page mode operation (EDO)

- Package and Ordering Information:
72-pin SIMM, order as
MB8504E032AA-xxSG
(SG = Gold Pad)
MB8504E032AA-xxSS
(SS = Solder Pad)

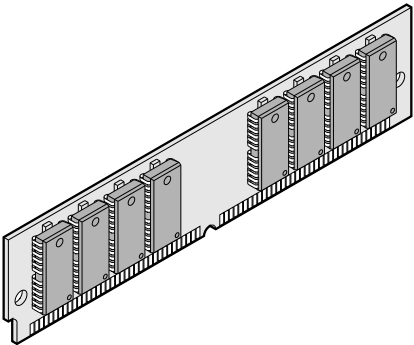
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■ PACKAGE

72-pin plastic SIMM (socket type)



(MSS-72P-P77)



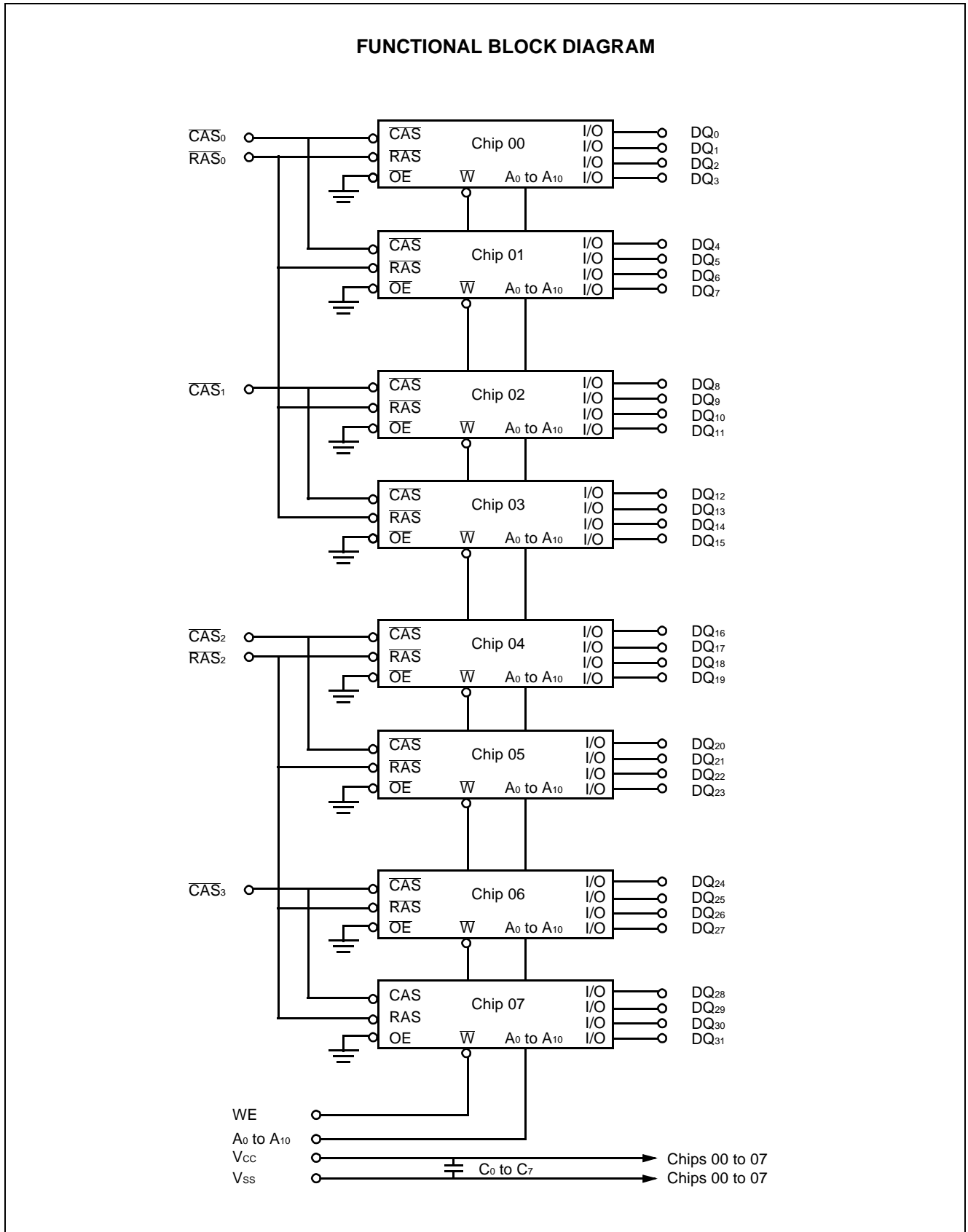
(MSS-72P-P79)

DQ ₀	2	1	V _{SS}
DQ ₁	4	3	DQ ₁₆
DQ ₂	6	5	DQ ₁₇
DQ ₃	8	7	DQ ₁₈
V _{CC}	10	9	DQ ₁₉
A ₀	12	11	N.C.
A ₂	14	13	A ₁
A ₄	16	15	A ₃
A ₆	18	17	A ₅
DQ ₄	20	19	A ₁₀
DQ ₅	22	21	DQ ₂₀
DQ ₆	24	23	DQ ₂₁
DQ ₇	26	25	DQ ₂₂
A ₇	28	27	DQ ₂₃
V _{CC}	30	29	N.C.
A ₉	32	31	A ₈
RAS ₂	34	33	N.C.
N.C.	36	35	N.C.
N.C.	38	37	N.C.
CAS ₀	40	39	V _{SS}
CAS ₃	42	41	CAS ₂
RAS ₀	44	43	CAS ₁
N.C.	46	45	N.C.
N.C.	48	47	WE
DQ ₂₄	50	49	DQ ₈
DQ ₂₅	52	51	DQ ₉
DQ ₂₆	54	53	DQ ₁₀
DQ ₂₇	56	55	DQ ₁₁
DQ ₂₈	58	57	DQ ₁₂
DQ ₂₉	60	59	V _{CC}
DQ ₃₀	62	61	DQ ₁₃
DQ ₃₁	64	63	DQ ₁₄
N.C.	66	65	DQ ₁₅
PD ₂	68	67	PD ₁
PD ₄	70	69	PD ₃
V _{SS}	72	71	N.C.

Pin #	Symbol	-60	-70
67	PD ₁	V _{SS}	V _{SS}
68	PD ₂	N.C.	N.C.
69	PD ₃	N.C.	V _{SS}
70	PD ₄	N.C.	N.C.

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FUNCTIONAL BLOCK DIAGRAM



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■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	-50 to +50	mA
Power Dissipation	P_D	8	W
Storage Temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITION

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, All Inputs*	V_{IL}	-0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

* : Undershoots of up to -2.0 volts with a pulse width not exceeding 10 ns are acceptable.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ CAPACITANCE

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{ V}$)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_{10}	C_{IN1}	—	71	pF
Input Capacitance, \overline{RAS}_0 and \overline{RAS}_3	C_{IN2}	—	39	pF
Input Capacitance, \overline{CAS}_0 to \overline{CAS}_3	C_{IN3}	—	23	pF
Input Capacitance, \overline{WE}	C_{IN4}	—	66	pF
I/O Capacitance, (DQ_0 to DQ_{31})	C_{DQ}	—	12	pF

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■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	Condition	Value		Unit
				Min.	Max.	
Output High Voltage	*1	V_{OH}	$I_{OH} = -5.0 \text{ mA}$	2.4	—	V
Output Low Voltage	*1	V_{OL}	$I_{OL} = 4.2 \text{ mA}$	—	0.4	V
Input Leakage Current	RAS	$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq V_{CC}$, $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, All other pins not under test = 0 V	-30	30	μA
	$\overline{\text{CAS}}$			-20	20	
	Address, WE			-60	60	
Output Leakage Current		$I_{O(L)}$	$0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V}$, Data out disabled	-10	10	μA
Operating Current (Average Power Supply Current)	*2	I_{CC1}	RAS & $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{min}$	—	840	mA
	MB8504E032AA-60			—	720	
Standby Current (Power Supply Current)		I_{CC2}	RAS = $\overline{\text{CAS}} = V_{IH}$ RAS = $\overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$	—	16	mA
	TTL Level			—	8	
Refresh Current#1 (Average Power Supply Current)	*2	I_{CC3}	$\overline{\text{CAS}} = V_{IH}$, RAS = cycling, $t_{RC} = \text{min}$	—	840	mA
	MB8504E032AA-60			—	720	
Hyper Page Mode Current	*2	I_{CC4}	RAS = V_{IL} , $\overline{\text{CAS}} = \text{cycling}$, $t_{HPC} = \text{min}$	—	720	mA
	MB8504E032AA-60			—	640	
Refresh Current#2 (Average Power Supply Current)	*2	I_{CC5}	RAS cycling, $\overline{\text{CAS}}$ -before-RAS, $t_{RC} = \text{min}$	—	840	mA
	MB8504E032AA-60			—	720	

Notes: *1. Referenced to V_{SS} .

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

I_{CC} depends on the number of address change as RAS = V_{IL} and $\overline{\text{CAS}} = V_{IH}$, $V_{IL} > -0.3 \text{ V}$.

I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} are specified at one time of address change during RAS = V_{IL} and $\overline{\text{CAS}} = V_{IH}$.

I_{CC2} is specified during RAS = V_{IH} and $V_{IL} > -0.3 \text{ V}$.

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■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB8504E032AA -60		MB8504E032AA -70		Unit
				Min.	Max.	Min.	Max.	
1	Time between Refresh		t _{REF}	—	32.8	—	32.8	ms
2	Random Read/Write Cycle Time		t _{RC}	104	—	124	—	ns
3	Access Time from $\overline{\text{RAS}}$	*4,7	t _{RAC}	—	60	—	70	ns
4	Access Time from $\overline{\text{CAS}}$	*5,7	t _{CAC}	—	15	—	17	ns
5	Column Address Access Time	*6,7	t _{AA}	—	30	—	35	ns
6	Output Hold Time		t _{OH}	3	—	3	—	ns
7	Output Hold Time from $\overline{\text{CAS}}$		t _{CHC}	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t _{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	*8	t _{OFF}	—	15	—	17	ns
10	Output Buffer Turn Off Delay Time from $\overline{\text{RAS}}$	*8	t _{OFR}	—	15	—	17	ns
11	Output Buffer Turn Off Delay Time from $\overline{\text{WE}}$	*8	t _{WEZ}	—	15	—	17	ns
12	Transition Time		t _T	1	50	1	50	ns
13	$\overline{\text{RAS}}$ Precharge Time		t _{RP}	40	—	50	—	ns
14	$\overline{\text{RAS}}$ Pulse Width		t _{TRAS}	60	100000	70	100000	ns
15	$\overline{\text{RAS}}$ Hold Time		t _{RSH}	15	—	17	—	ns
16	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t _{CRP}	5	—	5	—	ns
17	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Delay Time	*9,10	t _{RCO}	14	45	14	53	ns
18	$\overline{\text{CAS}}$ Pulse Width		t _{CAS}	10	—	13	—	ns
19	$\overline{\text{CAS}}$ Hold Time		t _{CSH}	40	—	50	—	ns
20	$\overline{\text{CAS}}$ Precharge Time (Normal)	*15	t _{CPN}	10	—	10	—	ns
21	Row Address Setup Time		t _{ASR}	0	—	0	—	ns
22	Row Address Hold Time		t _{RAH}	10	—	10	—	ns
23	Column Address Setup Time		t _{ASC}	0	—	0	—	ns
24	Column Address Hold Time		t _{CAH}	10	—	10	—	ns
25	Column Address Hold Time from $\overline{\text{RAS}}$		t _{AR}	24	—	24	—	ns
26	$\overline{\text{RAS}}$ to Column Address Delay Time	*11	t _{RAD}	12	30	12	35	ns
27	Column Address to $\overline{\text{RAS}}$ Lead Time		t _{RAL}	30	—	35	—	ns
28	Column Address to $\overline{\text{CAS}}$ Lead Time		t _{CAL}	23	—	28	—	ns
29	Read Command Setup Time		t _{RCS}	0	—	0	—	ns
30	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	*12	t _{RRH}	0	—	0	—	ns
31	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	*12	t _{RCH}	0	—	0	—	ns

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No.	Parameter	Notes	Symbol	MB8504E032AA -60		MB8504E032AA -70		Unit
				Min.	Max.	Min.	Max.	
32	Write Command Setup Time	*13	tWCS	0	—	0	—	ns
33	Write Command Hold Time		tWCH	10	—	10	—	ns
34	Write Command Hold Time from $\overline{\text{RAS}}$		tWCR	24	—	24	—	ns
35	$\overline{\text{WE}}$ Pulse Width		tWP	10	—	10	—	ns
36	Write Command to $\overline{\text{RAS}}$ Lead Time		tRWL	15	—	17	—	ns
37	Write Command to $\overline{\text{CAS}}$ Lead Time		tCWL	10	—	13	—	ns
38	DIN Setup Time		tDS	0	—	0	—	ns
39	DIN Hold Time		tDH	10	—	10	—	ns
40	Date Hold Time from $\overline{\text{RAS}}$		tDHR	24	—	24	—	ns
41	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh Cycles)		tRPC	5	—	5	—	ns
42	$\overline{\text{CAS}}$ Setup Time (C-B-R Refresh)		tCSR	0	—	0	—	ns
43	$\overline{\text{CAS}}$ Hold Time (C-B-R Refresh)		tCHR	10	—	12	—	ns
44	$\overline{\text{WE}}$ Setup Time from $\overline{\text{RAS}}$	*16	tWSR	0	—	0	—	ns
45	$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$	*16	tWHR	10	—	10	—	ns
46	$\overline{\text{RAS}}$ to Data In Delay Time		tRDD	15	—	17	—	ns
47	$\overline{\text{CAS}}$ to Data In Delay Time		tCDD	15	—	17	—	ns
48	DIN to $\overline{\text{CAS}}$ Delay Time		tDZC	0	—	0	—	ns
49	$\overline{\text{WE}}$ Precharge Time		tWPZ	8	—	8	—	ns
50	$\overline{\text{WE}}$ to Data In Delay Time		tWED	15	—	17	—	ns
51	Hyper Page Mode $\overline{\text{RAS}}$ Pulse Width		tRASP	—	100000	—	100000	ns
52	Hyper Page Mode Read/Write Cycle Time		tHPC	25	—	30	—	ns
53	Access Time from $\overline{\text{CAS}}$ Precharge	*7,14	tCPA	—	35	—	40	ns
54	Hyper Page Mode $\overline{\text{CAS}}$ Precharge Time		tCP	10	—	10	—	ns
55	Hyper Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge		tRHCP	35	—	40	—	ns

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- Notes:**
- *1. An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 μs is required after power-up followed by any eight \overline{RAS} -only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight \overline{CAS} - before- \overline{RAS} initialization cycles are required instead of eight \overline{RAS} cycles.
 - *2. AC characteristics assume $t_T = 5$ ns.
 - *3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
 - *4. Assumes that $t_{RCD} \leq t_{RCD}(\max)$, $t_{RAD} \leq t_{RAD}(\max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
 - *5. If $t_{RCD} \geq t_{RCD}(\max)$, $t_{RAD} \geq t_{RAD}(\max)$, and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC} .
 - *6. If $t_{RAD} \geq t_{RAD}(\max)$ and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
 - *7. Measured with a load equivalent to two TTL loads and 100 pF.
 - *8. t_{OFF} , t_{OFR} and t_{WEZ} are specified that output buffer change to high impedance state.
 - *9. Operation within the $t_{RCD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 - *10. $t_{RCD}(\min) = t_{RAH}(\min) + 2 t_T + t_{ASC}(\min)$.
 - *11. Operation within the $t_{RAD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 - *12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 - *13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}(\min)$ the data output pin will remain High-Z state through entire cycle.
 - *14. t_{CPA} is access time from the selection of a new column address (caused by changing \overline{CAS} from "L" to "H"). Therefore, if t_{CP} become long, t_{CPA} also become longer than $t_{CPA}(\max)$.
 - *15. Assumes that \overline{CAS} -before- \overline{RAS} refresh.
 - *16. Assumes that test mode function.

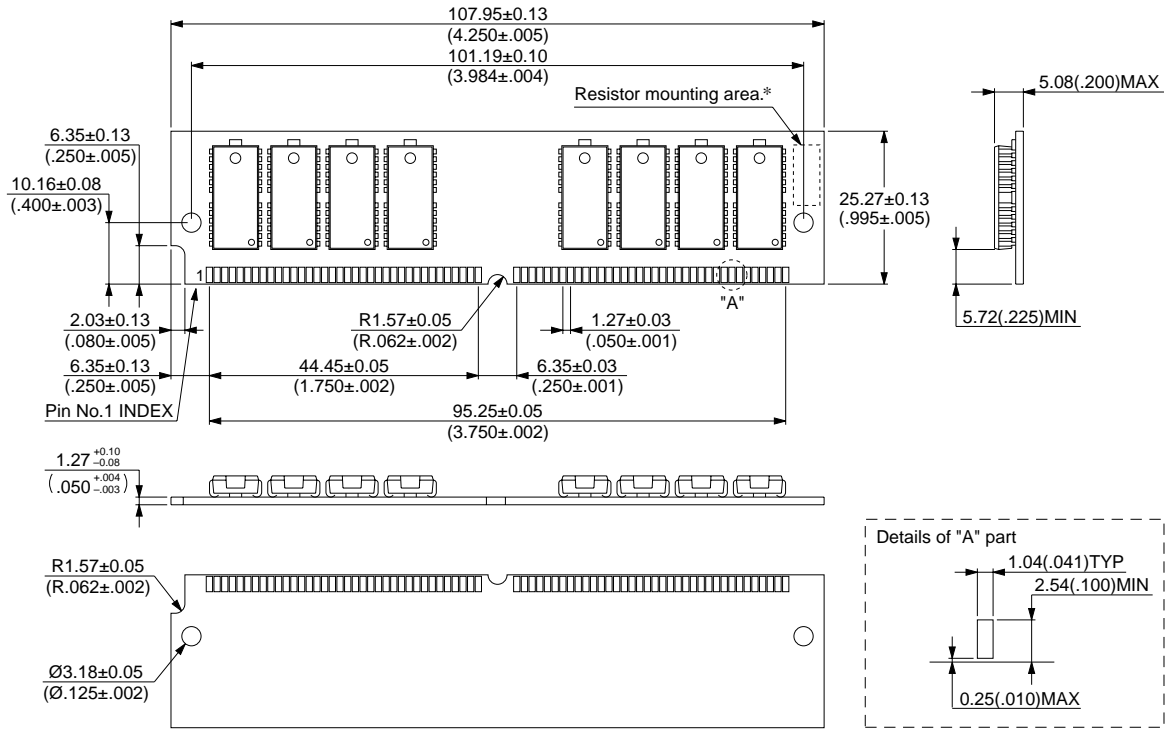
*Source: See MB8117405A Data Sheet for details on the electricals.

MB8504E032A-60/-70

■ PACKAGE DIMENSIONS

72-pin plastic SIMM (socket type)
(MSS-72P-P77)

* : Resistor thickness is 1.00 mm (.04 in.) maximum from board surface.



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Dimension in mm (inches)

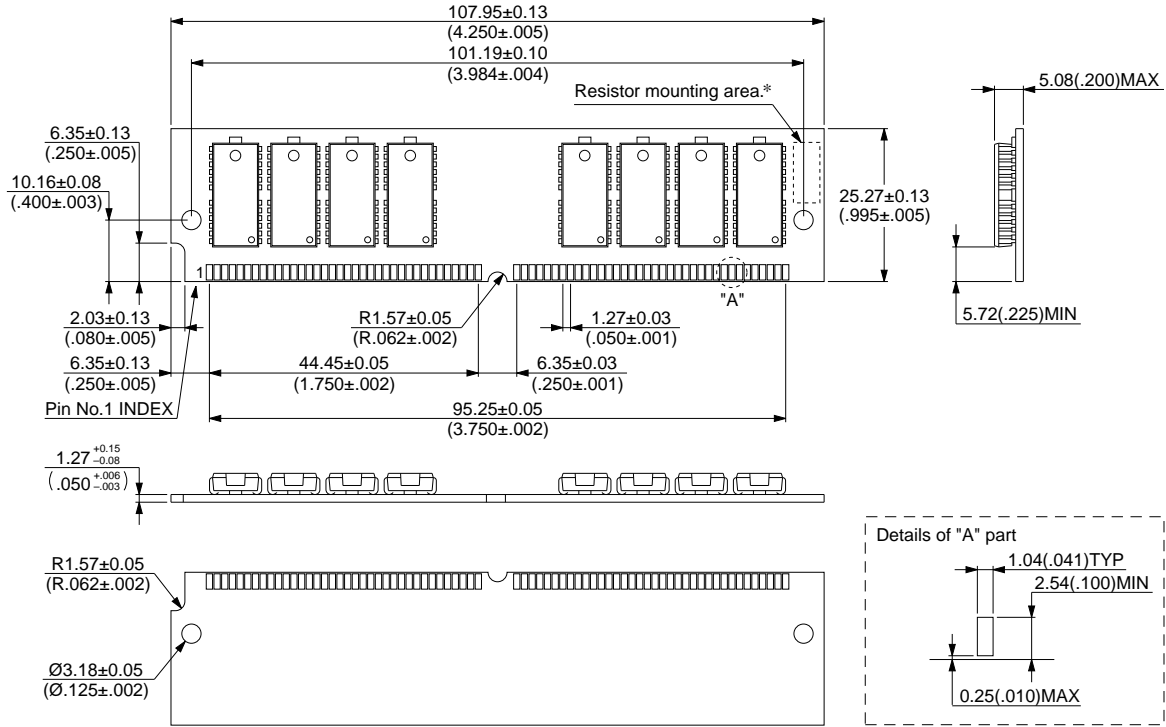
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72-pin plastic SIMM (socket type)
(MSS-72P-P79)

* : Resister thickness is 1.00 mm (.04 in.)
maximum from board surface.



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Dimension in mm (inches)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-8588, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

<http://www.fujitsu.co.jp/>

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: (800) 866-8608
Fax: (408) 922-9179

<http://www.fujitsumicro.com/>

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchsschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

<http://www.fujitsu-edc.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

<http://www.fmap.com.sg/>

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